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EXAMINER	
IWASHKO, LEV	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,127	FRANASZEK ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,12 and 27* is/are allowed.

6)☒ Claim(s) *1-10, 13-26 and 28-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 9-10, 13, 15-18 and 21 are rejected under U.S.C. 102(b) as being anticipated by Keltcher et al. (US Patent 6,314,494 B1).

Claim 1. A system for memory management, the system comprising a tag cache in communication with one or more cache devices in a storage hierarchy, wherein:

- the tag cache includes tags of recently accessed memory blocks, each tag corresponding to one of the memory blocks and each tag including tag contents; *(Column 1, lines 29-33 – State the following: "Instructions and data received from the main memory by the controller for execution are also stored in the high speed cache memory. Therefore, the controller has ready access to the most recently executed instructions and data if the same instructions or data be needed again by the controller." Column 1, lines 38-42 – State the following: "It is important to keep track of which lines of code and data are stored in the cache memory. One technique is to use TAG cache memory which includes memory locations for storing TAG addresses that correspond to addresses of the particular information stored in the cache memory")*
- the tag contents control which memory lines of the corresponding memory block are prefetched into at least one of the cache devices; *(Column 3, lines 11-32 – State the following: "As shown in the*

drawings for purposes of illustration, the invention is embodied in a size configurable data buffer. The size configurable data buffer includes two caches: data and prefetch. The size of the prefetch cache is adjustable. The size configurable data buffer can be implemented with a single SRAM (Static Random Access Memory) circuit. FIG. 1 shows an embodiment of the invention. This embodiment includes a size configurable data buffer 12. The size configurable data buffer 12 includes data cache and prefetch cache. Mask circuitry 14 determines the allocation between data cache and prefetch cache within the size configurable data buffer 12. The embodiment of FIG. 1 shows the data cache and prefetch cache within a single SRAM circuit, the size configurable data buffer 12. However, the data cache and prefetch cache can be divided into multiple SRAM circuits. A single SRAM circuit or integrated circuit is generally less expensive than two circuits or integrated circuits. The embodiment shown in FIG. 1 also includes an address recovery SRAM 16, a TAG SRAM 18, a TAG comparator 20, a controller (CPU) 22, a controller address bus (Controller Bus [31:0] 25), a main memory address bus (Main Memory BUS [31:0] 27) and a main memory 24")

- the tag contents are updated using a selected subset of processor references, said subset referred to as filtered references; and the tag contents are modified probabilistically at selected times or events. *(Column 6, lines 4-25 – State the following: "The store mode occurs when the controller 22 is writing new data to the size configurable data buffer 12 (data cache or prefetch cache). Initially, the CASTOUT input is deactivated (set false). The PREFETCH input is activated (set true) if the controller 22 recognizes the data as prefetch data. The controller 22 generates the address bits of the controller address bus 25 that correspond to the address of the location the data is to be written. When the address bits of the location match the line address*

bits stored within the address recovery SRAM 16 and the TAG address bits stored within the TAG SRAM 18, a TAG hit occurs and the controller 22 writes the data to the size configurable data buffer 12. When a TAG miss occurs and the data located in the size configurable data buffer 12 at the location the new data is to be written has previously been modified, then the controller 22 activates the CASTOUT input and transfers that data to the main memory 24. The controller then deactivates the CASTOUT line and writes the new data to the size configurable data buffer 12. Again, the PREFETCH input is activated when the controller 22 recognizes the data as prefetch data. The line address bits and the TAG address bits of the new data are stored in the address recovery SRAM 16 and the TAG SRAM 18 for future reference")

Claim 3. The system of claim 1 wherein the tag contents include a memory block real address and one bit for every memory line in the memory block, said bits referred to as prefetch bits. *(Column 4, lines 17-27 – State the following: "FIG. 3 shows the address bits of the Controller BUS 25 of FIG. 1. The address bits of the controller address bus 25 include column address bits 42, line address bits 44 and TAG address bits 46. This embodiment includes five column address bits (bits 4:0), seven line address bits (bits 11:5), and twenty TAG address bits (bits 31:12). Five column address bits are required because this embodiment of the size configurable data buffer 12 includes 32 columns. Seven line address bits are required because this embodiment of the size configurable data buffer 12 includes 128 lines (rows) of memory")*

Claim 9. The method of claim 3 wherein the tag contents include 32 prefetch bits. *(Column 4, lines 27-29 – State the following: "Twenty TAG address bits are required because in this embodiment the address bus 25 of the main memory 24 is thirty two bits wide")*

Claim 10. The system of claim 3 wherein the value of each prefetch bit determines whether the corresponding memory line should be prefetched. *(Column 4, lines 33-43 – State the following: "The mask circuitry 14 modifies the line address bits (Controller BUS [11:5]) of the Controller BUS 25 under certain conditions. The mask circuitry 14 generates Line Address [6:0] that correspond to the seven Controller BUS [11:5] bits or the modified line address bits. The mask circuitry 14 receives a Prefetch input and a CASTOUT input. When the Prefetch input is active (high) and the CASTOUT input is inactive (low), the mask circuitry 14 modifies the line address bits by "anding" the line address bits with the mask lines 15. The controller 22 controls the Prefetch input, the CASTOUT input and the mask lines 15")*

Claim 13. The system of claim 1 wherein an access by one of the cache devices to a memory line corresponding to one of the prefetch bits results in the prefetch bit not being reset to a nonprefetch status before the tag is stored back to the memory device. *(Column 5, lines 32-34 – State the following: "When the controller 22 specifies the requested data as prefetch data, the PREFETCH input is activated (set true) by the controller")*

Claim 15. The system of claim 1 wherein each of the memory blocks is four thousand and ninety-six (4K) bytes, each of the memory blocks includes 32 memory lines, and each of the memory lines is 128 bytes. *(Column 3, lines 50-66 – State the following: "FIG. 2 shows a memory allocation representation of the size configurable data buffer 12 which includes data cache 32 and prefetch cache 34. For this embodiment, the size configurable data buffer 12 includes 128 lines of information. Each line is divided into 32 columns of 8 bits of data. Therefore, the size configurable data buffer 12 of this embodiment is 256 bits wide. Since the size configurable data buffer 12 of the embodiment of the invention described here includes 128 lines and 32 columns, the configurable data buffer 12 can include an desired number of lines and columns. The size of the*

support circuitry (the mask circuitry 14, the address recovery SRAM 16, the TAG SRAM 18) will vary accordingly. The number of address line includes within the Controller BUS 25 and the main Main Memory BUS 27 can also vary. Since the size configurable data buffer 12 includes data cache 32 and prefetch cache 34. Therefore, adjustment of the size of the prefetch cache 34 will affect the size of the data cache 32")

Claim 16. The system of claim 1 wherein the prefetch occurs when a filtered reference event occurs and the tag cache does not contain an entry for the corresponding memory block. *(Column 6, lines 15-24 – State the following: "When a TAG miss occurs and the data located in the size configurable data buffer 12 at the location the new data is to be written has previously been modified, then the controller 22 activates the CASTOUT input and transfers that data to the main memory 24. The controller then deactivates the CASTOUT line and writes the new data to the size configurable data buffer 12. Again, the PREFETCH input is activated when the controller 22 recognizes the data as prefetch data")*

Claim 17. The system of claim 1 wherein an access by one of the cache devices to one of the memory lines results in the prefetch bit corresponding to the memory line not being reset to a nonprefetch status before the tag is stored back to the memory device if the access passes filtering criteria. *(Column 5, lines 27-30 – State the following: "The controller can subsequently utilize the data from the size configurable data buffer 12 that was accessed at the same time as the TAG access")*

Claim 18. The system of claim 1 wherein the tags are returned to the memory device when the tag is deleted from the tag cache. *(Column 6, lines 15-24 – State the following: "When a TAG miss occurs and the data located in the size configurable data buffer 12 at the location the new data is to be written has previously been modified, then the controller 22 activates the CASTOUT input and transfers that data to the main memory 24. The controller then deactivates the CASTOUT line and writes the new data to*

the size configurable data buffer 12. Again, the PREFETCH input is activated when the controller 22 recognizes the data as prefetch data")

Claim 21. The system of claim 1 wherein the memory block is a system page. *(Figure 2 – Shows a memory block)*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 22 is rejected under 35 U.S.C.103(a) as being unpatentable over Keltcher, further in view of Dean (US Patent 5,544,342).

Keltcher teaches the limitations of claim 22 as follows:

- prefetching the memory lines corresponding to the prefetch bits in the tag that are set to a prefetch status, said prefetching into the cache device; *(Column 3, lines 11-32 – State the following: "As shown in the drawings for purposes of illustration, the invention is embodied in a size configurable data buffer. The size configurable data buffer includes two caches: data and prefetch. The size of the prefetch cache is adjustable. The size configurable data buffer can be implemented with a single SRAM (Static Random Access Memory) circuit. FIG. 1 shows an embodiment of the invention. This embodiment includes a size configurable data buffer 12. The size configurable data buffer 12 includes data cache and prefetch cache. Mask circuitry 14 determines the allocation between data cache and prefetch cache within the size configurable data buffer 12. The embodiment of FIG. 1 shows the data cache and prefetch cache within a single SRAM circuit, the size configurable data buffer 12. However, the data cache and prefetch cache can be divided into multiple SRAM circuits. A single SRAM circuit or integrated circuit is generally less expensive than two circuits or integrated circuits. The embodiment shown in FIG. 1 also includes an address recovery SRAM 16, a TAG SRAM 18, a TAG comparator 20, a controller (CPU) 22, a controller address bus*

(Controller Bus [31:0] 25), a main memory address bus (Main Memory BUS [31:0] 27) and a main memory 24")

- and resetting each of the prefetch bits which were set to a prefetch status to a nonprefetch status with a selected probability; *(Column 5, lines 32-37 – State the following: "When the controller 22 specifies the requested data as prefetch data, the PREFETCH input is activated (set true) by the controller. Otherwise, the PREFETCH input is not activated (set false). As previously stated, when the PREFETCH input is true and the CASTOUT input is false, the line address bits are modified by the mask circuitry 15")*
- determining if a tag corresponding to the fault memory block is present in a tag cache, wherein the tag includes prefetch bits corresponding to memory lines contained in a memory block specified by the tag; *(Column 5, lines 18-31 – State the following: "The TAG comparator 20 compares address bits of the controller address bus 25 (line address and TAG address bits) of data requested by the controller 22 with the address bits of the main memory address bus 27 (line address and TAG address bits) stored in the corresponding address recovery SRAM 16 and TAG SRAM 18 line address or modified line address locations. When f the requested address bits and the stored address bits are identical, a TAG hit occurs that indicates to the controller 20 that the requested data is stored in the data cache or the prefetch cache of the size configurable data buffer 12. The controller can subsequently utilize the data from the size configurable data buffer 12 that was accessed at the same time as the TAG access. If a TAG miss occurs, the controller must access the requested data from the main memory 24")*

Keltcher's invention differs from the claimed invention in that there is no specific reference to faults.

Keltcher fails to teach the entirety of Claim 22. However, Dean teaches the following aspects of Claim 22:

A method for memory management, the method comprising:

- receiving a notification of a cache fault from a cache device, the notification including a fault memory block and a fault memory line; *(Column 31, lines 57-60 – State the following: "For fetch-on-fault, a fetch to the next level in the memory hierarchy is initiated in response to a cache miss and retrieves more than one cache block of data (fetch size >block size)")*

- in response to not locating the tag corresponding to the fault memory block in the tag cache: fetching the tag corresponding to the fault memory block into the tag cache; *(Column 32, lines 1-4 – State the following: "For tagged-sequential prefetching, a fetch to the next level in the memory hierarchy is initiated in response to a processor request to a cache block which has been fetched but not accessed by the processor")*
- and setting the prefetch bit corresponding to the fault memory line in the tag to the prefetch status. *(Column 31, lines 60-62 – State the following: "The additional blocks or subblocks of fetched data are sequentially addressed from the cache miss block address")*

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Dynamically Size Configurable Data Buffer for Data Cache and Prefetch Cache Memory" of Keltcher and Dean's "System and Method For Prefetching Information in a Processing System" before him at the time the invention was made, to combine the inventions to utilize faults in order to make the system more efficient and diminish error handling problems.

4. Claim 23 is rejected under 35 U.S.C.103(a) as being unpatentable over Keltcher, further in view of Dean (US Patent 5,544,342) and Ellis et al. (US Patent 5,418,973).

Keltcher and Dean teach the limitations of claim 22 for the reasons above.

Keltcher and Dean's inventions differ from the claimed invention in that there is no specific reference to virtual memory.

Keltcher and Dean fail to teach claim 23, which states the following: "The method of claim 22 wherein the tag further includes a next virtual memory block bit and the method further comprises prefetching selected lines of the next virtual memory block into the cache device in response to: not locating the tag corresponding to the fault memory block and the next virtual memory block in the tag cache; and the next virtual memory block bit being set to a prefetch status." However, Ellis's invention discloses the following: "Then the microcode begins

controlling the execution unit to sequentially compute virtual memory addresses of the vector elements, beginning with a base address, which is successively incremented by the stride of the vector. These memory addresses are also passed through the pipeline, but the address for a masked reference is blocked at the E-M latch, and any element following the last element of the vector is also blocked at the E-M latch" (column 13, lines 41-50). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Dynamically Size Configurable Data Buffer for Data Cache and Prefetch Cache Memory" of Keltcher, Dean's "System and Method For Prefetching Information in a Processing System", and Ellis' "Digital Computer System with Cache Controller" before him at the time the invention was made, to combine the inventions to utilize virtual memory in order to provide the computer with more memory options making the system faster and more useful.

5. Claims 2, 4-6, and 24-26 are rejected under 35 U.S.C.103(a) as being unpatentable over Keltcher and Dean as applied to claims 1, 3, and 22-23, further in view of Ellis et al. (US Patent 5,418,973).

Keltcher and Dean teach the limitations of claims 1, 3, and 22-23 for the reasons above.

Keltcher and Dean's inventions differ from the claimed invention in that there is no specific reference to virtual memory.

Keltcher and Dean fail to teach claims 2, 4-6, and 24-26, which state as follows:

Claim 2. The system of claim 1 wherein the tag contents further control which next virtual memory block is prefetched into at least one of the cache devices.

Claim 4. The system of claim 3 wherein the tag contents further include a bit to control prefetching of memory lines from a next virtual memory block, said bit referred to as a next virtual memory block bit.

Claim 5. The system of claim 4 wherein the next virtual memory block bit in a preceding memory block in a virtual address space is set to a prefetch status when the preceding memory block tag is in the tag cache.

Claim 6. The system of claim 4 wherein the next virtual memory block bit is turned to a nonprefetch status with a specified probability on certain events.

Claim 24. The method of claim 23 wherein the prefetching selected lines of the next virtual memory block includes prefetching the memory lines corresponding to the prefetch bits set to a prefetch status in the tag corresponding to the next virtual memory block.

Claim 25. The method of claim 23 wherein the next virtual memory block bit in a preceeding memory block in a virtual address space is set to a prefetch status when the preceeding memory block tag is in the tag cache.

Claim 26. The method of claim 23 wherein the next virtual memory block bit is turned to a nonprefetch status with a specified probability on certain events.

However, Ellis's invention discloses the following: "Then the microcode begins controlling the execution unit to sequentially compute virtual memory addresses of the vector elements, beginning with a base address, which is successively incremented by the stride of the vector. These memory addresses are also passed through the pipeline, but the address for a masked reference is blocked at the E-M latch, and any element following the last element of the vector is also blocked at the E-M latch" (column 13, lines 41-50). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Dynamically Size Configurable Data Buffer for Data Cache and Prefetch Cache Memory" of Keltcher, Dean's "System and Method For Prefetching Information in a Processing System", and Ellis' "Digital Computer System with Cache Controller" before him at the time the invention was made, to combine the inventions to utilize virtual memory in order to provide the computer with more memory options making the system faster and more useful.

6. Claim 7 is rejected under 35 U.S.C.103(a) as being unpatentable over Keltcher and Dean as applied to claims 1, 3-4, and 6, further in view of Ellis et al. (US Patent 5,418,973).

Keltcher, Dean and Ellis teach the limitations of claims 1, 3-4, and 6 for the reasons above.

Claim 7 reads as follows: "The system of claim 6 wherein the certain events include eviction of the tag from the tag cache."

Keltcher teaches the limitations of Claim 7 as follows: "When a TAG miss occurs and the data located in the size configurable data buffer 12 at the location the new data is to be written has previously been modified, then the controller 22 activates the CASTOUT input and transfers that data to the main memory 24. The controller then deactivates the CASTOUT line and writes the new data to the size configurable data buffer 12. Again, the PREFETCH input is activated when the controller 22 recognizes the data as prefetch data" (Column 6, lines 15-24).

Claim 7 is rejected based on the same grounds as Claim 18, but due to Claim 7's dependence on Claim 6, a 103(a) rejection necessitated use.

7. Claims 8 and 19-20 are rejected under 35 U.S.C.103(a) as being unpatentable over Keltcher as applied to claims 1 and 3, further in view of Dean (US Patent 5,544,342).

Keltcher teaches the limitations of claims 1 and 3 for the reasons above.

Keltcher's invention differs from the claimed invention in that there is no specific reference to L1 and L2 caches.

Keltcher fails to teach claims 8 and 19-20, which state as follows:

Claim 8. The system of claim 3 wherein: one of the cache devices is a level two cache device and another is a level one cache device; the prefetch bits are set by a selected subset of misses from the level one cache device; and the misses include at least one miss from the level two cache device.

Claim 19. The system of claim 1 wherein one of the cache devices is a level one cache device.

Claim 20. The system of claim 1 wherein one of the cache devices is a level two cache device.

However, Dean's invention discloses the following: "First-Level Cache: According to the preferred embodiment, a first-level cache is also called the primary cache. In conventional

system structures, the first-level cache is the first storage layer in the memory system hierarchy. Many advanced processor chips include internal first-level caches which range in size from 1K words to 4K words. By comparison, in the STRiP architecture of the preferred embodiment, the first-level instruction and data caches are the second layer in the memory hierarchy" (Column 64, lines 42-51). "Second-Level Cache: In a multi-level cache hierarchy, the second-level cache is located beyond the first-level cache. In the preferred embodiment, the second-level cache ranges in size from 16K words to 512K words. Second-level caches are normally formed by discrete SRAMs. Second-level caches are also refererred to as secondary caches? (Column 64, lines 52-59). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Dynamically Size Configurable Data Buffer for Data Cache and Prefetch Cache Memory" of Keltcher and Dean's "System and Method For Prefetching Information in a Processing System" before him at the time the invention was made, to combine the inventions to utilize L1 and L2 caches to allow the system to be more versatile.

8. Claim 14 is rejected under 35 U.S.C.103(a) as being unpatentable over Keltcher as applies to claim 1, further in view of Ellis et al. (US Patent 5,418,973)

Keltcher teaches the limitations of claim 1 for the reasons above.

Keltcher's invention differs from the claimed invention in that there is no specific reference to sending of the entries from the one or more cache devices to storage hierarchies of other processors.

Keltcher fails to teach claim 14, which states the following: "The system of claim 1 wherein the tag contents further control the sending of the entries from the one or more cache devices to storage hierarchies of other processors." However, Ellis's invention discloses the

following: "A valid, dirty, and shared bit are associated with each tag in the write-back cache (44 in FIG. 4), and are read from the cache with the tag and sent to the cache controller 77 via a bus 138 together with a "tag ok" signal on a line 139. In a multi-processor system, the valid and shared bits are written by the cache in response to fills from the main memory (45 in FIG. 4) and cache coherency commands from other processors (not shown)" (Column 16, lines 30-37). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Dynamically Size Configurable Data Buffer for Data Cache and Prefetch Cache Memory" of Keltcher and Ellis "Digital Computer System with Cache Controller" before him at the time the invention was made, to combine the inventions to be able to send entries from the one or more cache devices to storage hierarchies of other processors so that the system would be more universal and user-friendly.

9. Claims 28-31 are rejected under 35 U.S.C.103(a) as being unpatentable over Keltcher as applies to claim 22, further in view of Dean (US Patent 5,544,342).

Claims 28-31 are rejected on the same grounds as Claims 13, 17-18 and 21 respectively, as they all disclose the same material with the exception of the material disclosed in the independent Claim 22.

10. Claim 32 is rejected under 35 U.S.C.103(a) as being unpatentable over Keltcher, further in view of Dean (US Patent 5,544,342).

Claim 32 is rejected on the same grounds as Claim 22, as it discloses the same material with the exception of the program, which is disclosed in Dean: "The average access time of a memory system depends on many factors: the processor's architecture, the program's behavior, the caches' sizes and organizations, and the fetch and prefetch strategies" (Column 16, lines 21-

25). Therefore, it would have been obvious to combine Keltcher and Dean's inventions to include a program so that the system would be operational on a digital level, thereby making it more useful and efficient.

Allowable Subject Matter

11. Claims 11-12 and 27 are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claim 11 states that there is a selected probability of between zero and one. This claim is very specific, cannot be overcome with prior art, and therefore warrants allowability.

Claims 12 and 27 both state that the selected probability is one eighth. These claims are very specific, cannot be overcome with prior art, and therefore warrant allowability.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW KIM
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